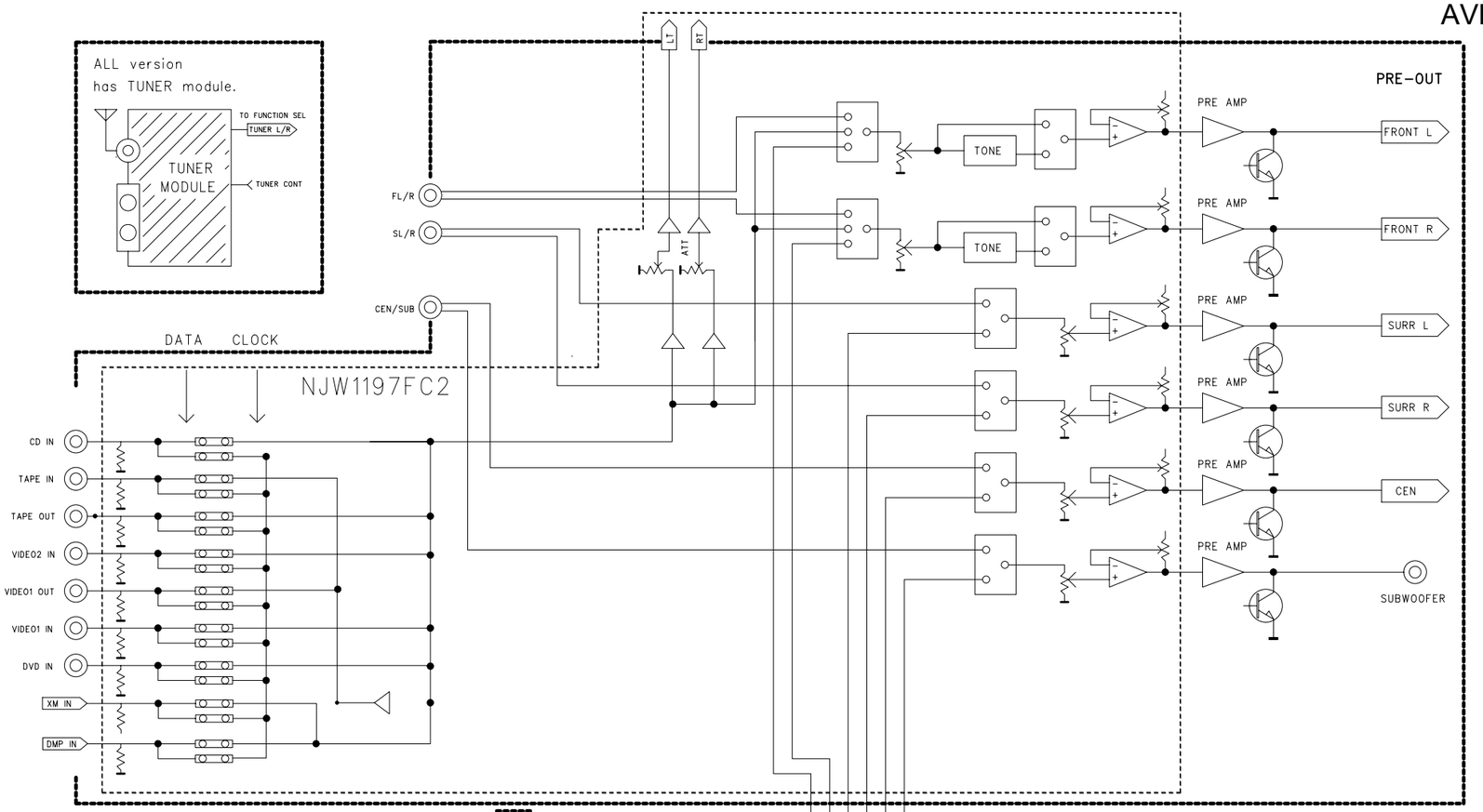
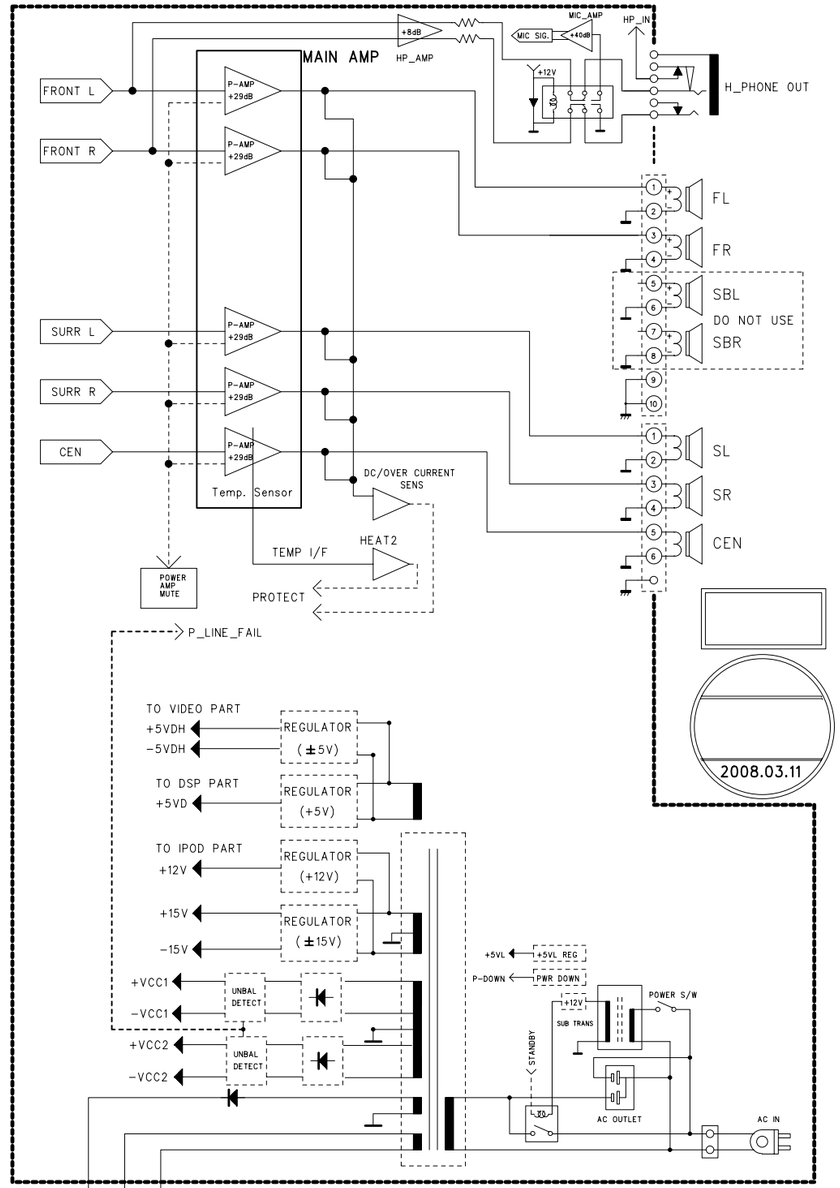
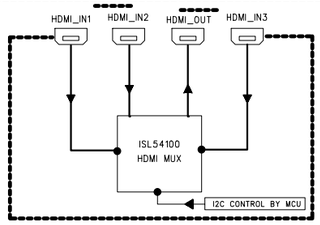
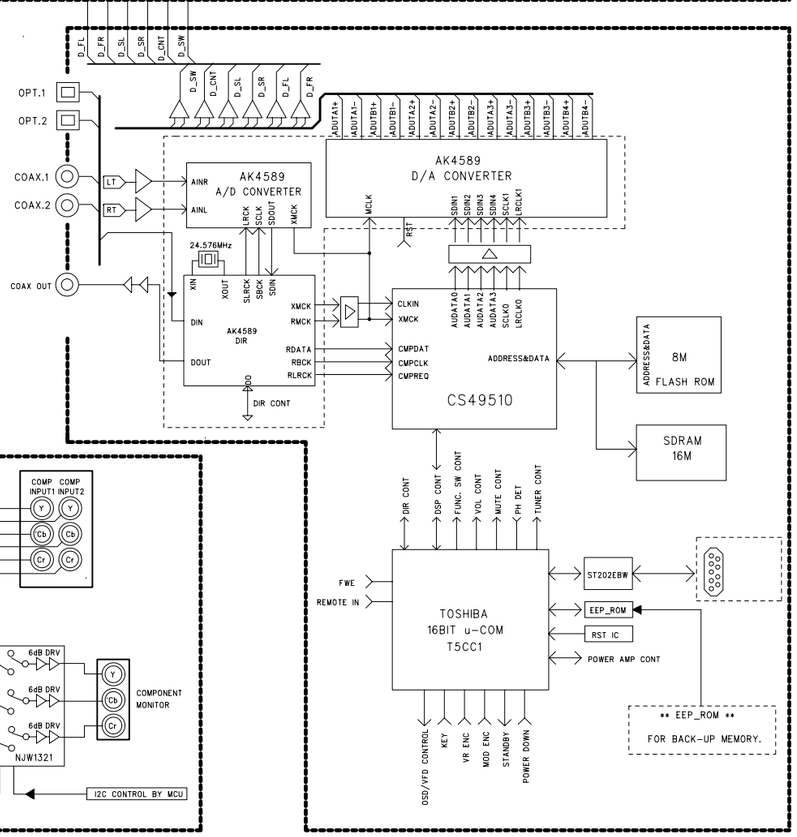
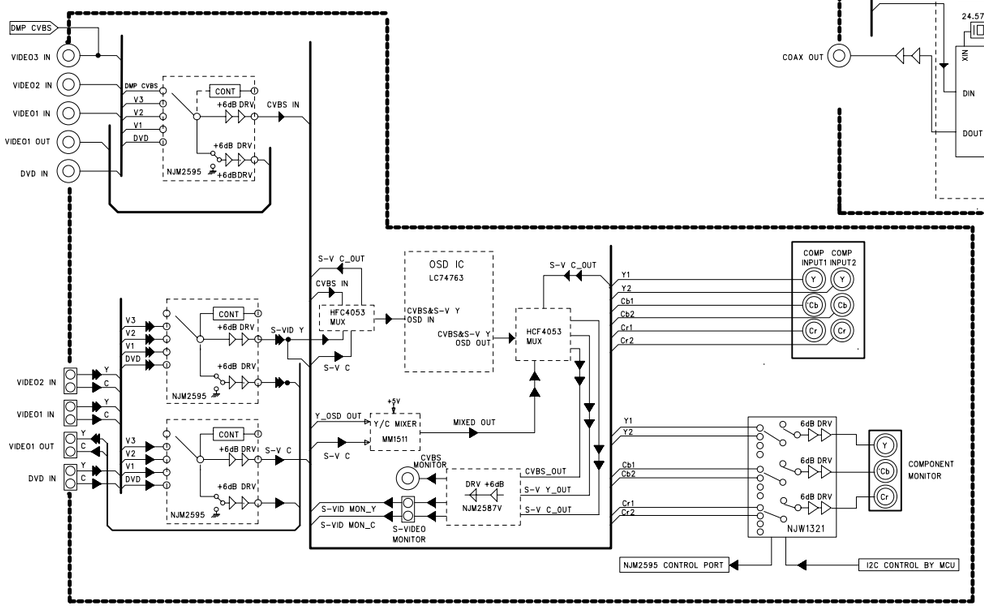
AVR154 BLOCK DIAGRAM

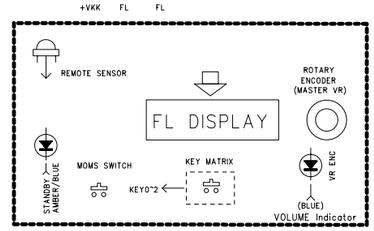


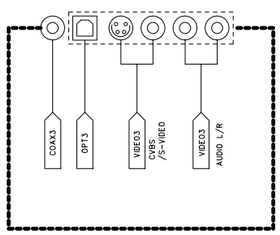


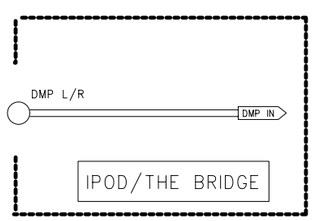








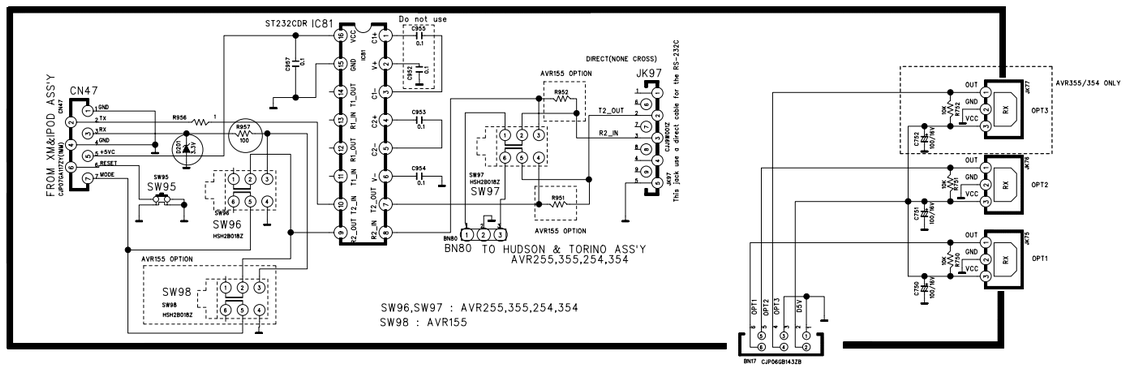




REVISION	2		4		6	
1		3		5		7

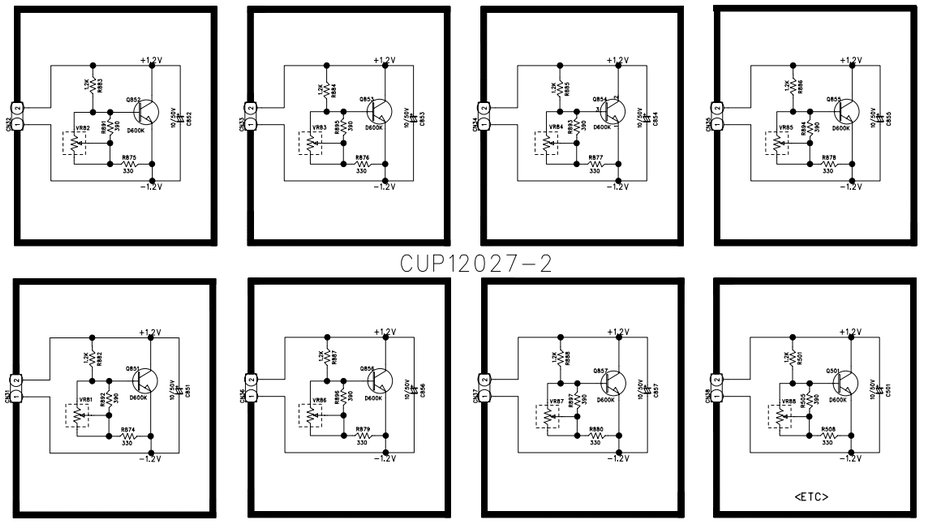
			SHEET 1/1
MODEL			
DESIGN	CHECK	APPROVE	DRAWING NO
J.T.BAEK		K.S.WEY	BLOCK DIAGRAM 1/1
	08.03.11	08.03.11	

CUP12027-1

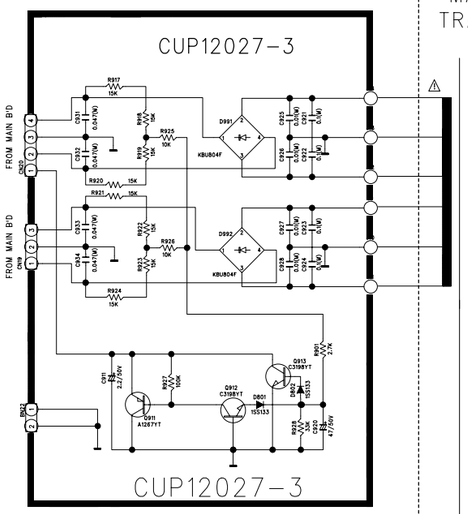


< OPTICAL IN & RS-232 PCB >

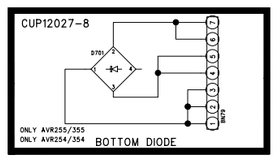
< BIAS T.R PCB >



CUP12027-3

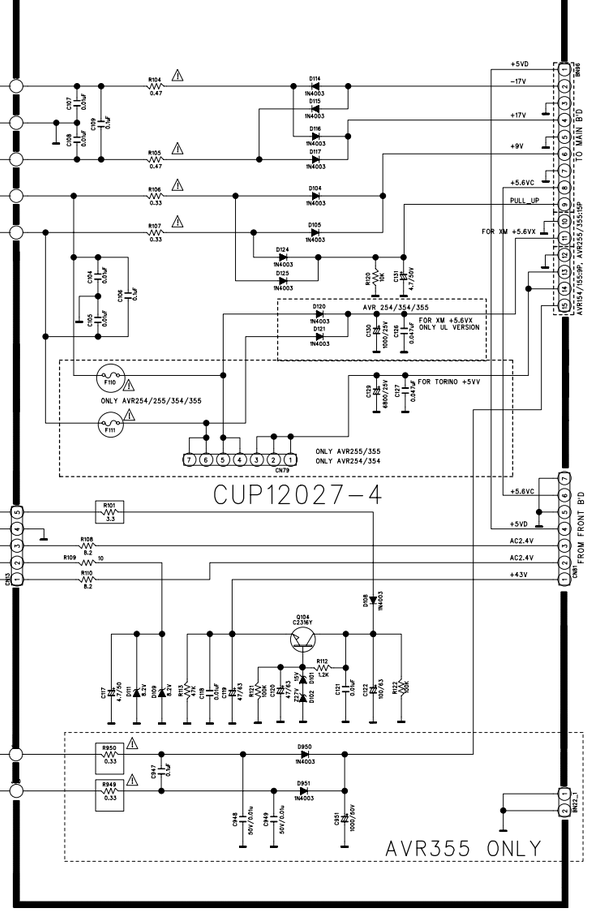


CUP12027-3

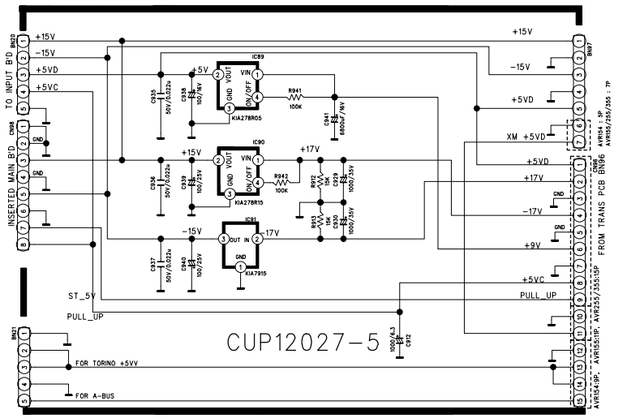


USA : AC120V 60Hz
EUR : AC230V 50Hz

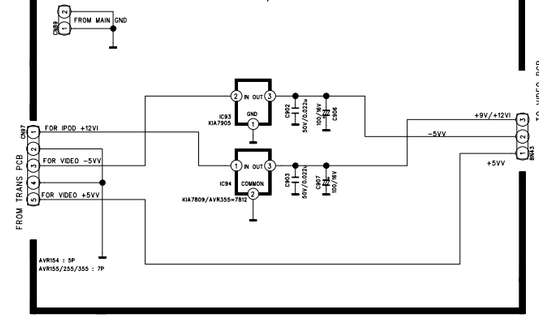
MAIN TRANS



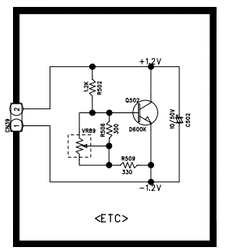
< TRANS PCB >

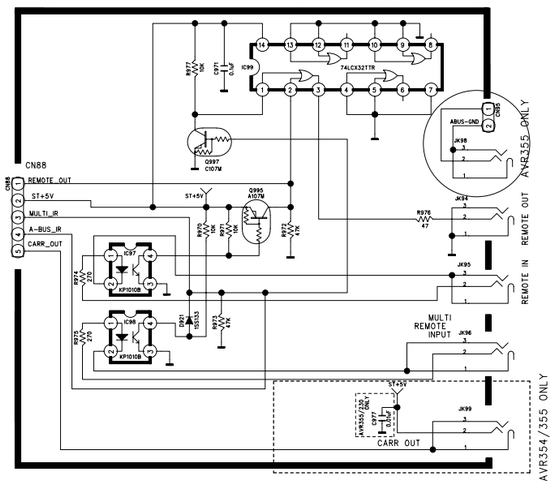


CUP12027-6 ONLY AVR154/155 USE



< REGULATOR PCB >





AVR254/255/354/355 ONLY CUP12027-7

< REMOTE IN/OUT PCB >

M P

SUE
2008.01.2

REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM — SHEET 1/1

MODEL	AVR x54/x55		
DESIGN	CHECK	APPROVE	DRAWING NO
J.T.B	Y.Y.W	K.S.W	CUP12027Z (POWER)
08.01.22			1/1

R201 ~ R216 : 470 Ohm-->100 Ohm
R219 ~ R223 : 470 Ohm-->100 Ohm
R225 ~ R226 : 470 Ohm-->100 Ohm

CD
R/O
TAPE
P/B
VIDEO3
AVR154/155 No Need
VIDEO2
R/O
VIDEO1
P/B
DVD
8CH Lch
8CH Rch
8CH SLch
8CH SRch
8CH Cch
8CH SUB
8CH SBL
8CH SBR
AVR154/155 No Need

From FRONT INPUT CN10
MIC SIGNAL
CVNJM1197CFC2
IC20
AVR155(UL) ONLY
AVR154(UL) AVR154/155(EUR) ONLY

VOL(01-08)

D_FL- D_FL+ D_FR+ D_FR- D_CT- D_CT+ D_SW+ D_SW- D_SL- D_SL+ D_SR+ D_SR- D_BL- D_BL+ D_BR+ D_BR-

IC31 IC21 IC32 IC22 IC33 IC23 IC34 IC24

DAC-L DAC-R DAC-C DAC-SW DAC-SL DAC-SR DAC-BL DAC-BR

VOL01 VOL-L VOL02 VOL-R VOL03 VOL-C VOL04 VOL-SL VOL05 VOL-SR VOL06 VOL-BL VOL07 VOL-BR VOL08 VOL-SW

HPL-OUT HPR-OUT L-OUT R-OUT C-OUT SW-OUT SL-OUT SR-OUT SBL-OUT SBR-OUT

FUNC_MUTE2 SB_MUTE2

FROM CONNECT B'D
DGND
FROM TUNER MODULE
FROM REG. B'D

IC36 HV7A1780BAPI (+12V)
IC37 CVKA7905PI (-12V)

** IMPORTANT SAFETY NOTICS.
COMPONENTS IDENTIFIED BY ⚠ MARK HAVE SPECIAL CHARACTERISTICS.
IMPORTANT FOR SAFETY. WHEN REPLACING ANY OF THESE COMPONENTS
USE ONLY MANUFACTURER'S SPECIFIED PARTS.
** THE UNIT OF RESISTANCE IS OHM.
K=1000 OHM , M=1000 KOHM
** THE UNIT OF CAPACITANCE IS MICROFARAD. (uF)
pF=10^{-6} uF
** THIS SCHEMATIC DIAGRAM MAY MODIFIED AT ANY TIME WITH THE
IMPROVEMENT OF PERFORMANCE.

REVISION	2	4	6	
1	3	5	7	

SCHEMATIC DIAGRAM — SHEET 1/3

MODEL	AVR154/155	
DESIGN	CHECK	APPROVE	DRAWING NO
C.B.LEE	W.Y.YANG	G.S.WEY	2028SCLZ (INPUT) 1/1
07.05.28			

CUP12028Z

ADC MODE : DSP MASTER
DIR MODE : DIR MASTER

CRJ10DJ1R0T

CRJ10DJ301T

HVIAK4589VQ-T

CD49500/10

pin 25 <--> pin28

*OPTION : EMC COUNTERMEASUER

DATA	CS495**	Flash	SDRAM
EXT_D15/SD_D7	29	44	12
EXT_D14/SD_D6	30	42	11
EXT_D13/SD_D5	31	40	9
EXT_D12/SD_D4	32	38	8
EXT_D11/SD_D3	34	35	6
EXT_D10/SD_D2	35	33	5
EXT_D9/SD_D1	37	31	3
EXT_D8/SD_D0	39	29	2
EXT_D7/SD_D15	40	45	49
EXT_D6/SD_D14	41	43	48
EXT_D5/SD_D13	42	41	46
EXT_D4/SD_D12	43	39	45
EXT_D3/SD_D11	45	36	43
EXT_D2/SD_D10	46	34	42
EXT_D1/SD_D9	48	32	40
EXT_D0/SD_D8	49	30	39

Address	CS495**	Flash	SDRAM
EXT_A19	88	9	
EXT_A18	87	16	
EXT_A17	85	17	
EXT_A16	84	48	
EXT_A15	82	1	
EXT_A14/SD_A13	77	3	
EXT_A13/SD_A14	75	2	
EXT_A12/SD_A10	74	6	20
EXT_A11/SD_A12	55	4	
EXT_A10/SD_A11	56	5	19
EXT_A9/SD_A9	58	7	32
EXT_A8/SD_A8	59	8	31
EXT_A7/SD_A7	61	18	30
EXT_A6/SD_A6	62	19	29
EXT_A5/SD_A5	64	20	28
EXT_A4/SD_A4	67	21	27
EXT_A3/SD_A3	68	22	24
EXT_A2/SD_A2	70	23	23
EXT_A1/SD_A1	71	24	22
EXT_A0/SD_A0	72	25	21

REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM — SHEET 2/3

MODEL	AVR154/155	
DESIGN	CHECK	APPROVE	DRAWING NO
C.B.LEE	W.Y.YANG	G.S.WEY	2028SCLZ (DSP) 1/1
07.05.28			

TO VIDEO PCB

CN4 CUP130A1UTZV

OSD_M_VHS_SCL
OSD_2M_VHS_SDA
OSD_CS1
COMP_IN_CHECK
1317/RHS_SCLK
1317/RHS_SDA
OSD_M/1080A_INPUT
PDO_Y_SEL

CUP12028-2

RDS SECTION(EUR Ver. ONLY)

+5VD
GND
MPX_OUT
RDS_CLK
RDS_DATA

TO FRONT PCB

CN77

POWER_HIGH
MIC_IN
VOL_L_CONT
KEY1
KEY2
KEY3
VOL_EN1
VOL_EN2
VFD_CS
VFD_CLK
VFD_DATA
VFD_RST
HP_IN
HP_MUTE2
REMOTE_IN

TO XM& IPOD PCB

AVR154 : 7P
AVR155 : 11P

CN78

XM_RST
XM_TX
XM_RX
DMP_DET
PC/DMP_TX
PC/DMP_RX
4384_RST

AVR-154

Update: LOW

155 Only

+OPTION B

OPTION B

SPEAKER A
SPEAKER B
XM_MUTE
XM_CMD
XM_IRQ

IC90
T5CC1

OPEN DRAIN
MULTI_IR

OPTION A

OPTION C

CARR_OUT

1159_DATA
1159_CLK
1159_LATCH
PROTECT_IN

MEV_STB
DSP_RESET
SCPI_BSY
DSPDATA
SCPI_CS
SCPI_SDA
DSPCLK
SCPI_IRQ
D_OUT
AKCE
AKRESET
1197_DATA
1197_CLK
1197_LATCH
1197_MUTE

R711 : RDS ON
+OPTION
R712 :RDS OFF

FUNC_MUTE1
FUNC_MUTE
HP_MUTE1
HP_MUTE

SB_MUTE2
P_FAIL
PROTECT_IN
HP_MUTE2
FUNC_MUTE2
POWER_DOWN
POWER_HIGH
POWER_MUTE
HP_MUTE1
FUNC_MUTE1

IC87 HVIRESVT28CATZ
(2.8V RESET)

RESET IN

IC89
CVIM24C32WMN6TP

REMOTE_IR
RDS_CLK
POWER_DOWN
T_DOUT
TUNED
STEREO
RDS_DATA
P_FAIL

T_CE
T_DATA
T_CLK

IC88
CVIA1A1117533

CUP12028-3
ST+5V REG PCB

IC84
CVIA1A1117550

TO MAIN PCB

○: PULL_UP
GPIO : Input/Out Port(without pull_up resistor)

* MODEL OPTION

MODEL	OP_A(PIN48)	OP_B(PIN98)	OP_C(PIN52)
AVR155	HIGH(R792)	LOW(R791)	LOW(R712)
AVR154	HIGH(R792)	HIGH(R790)	LOW(R712)
AVR155/230	LOW(R793)	LOW(R791)	HIGH(R711)
AVR154/230	LOW(R793)	HIGH(R790)	HIGH(R711)

REVISION	2	4	6	
1	3	5	7	

SCHEMATIC DIAGRAM — SHEET 1/3

MODEL	AVR154/155	
DESIGN	CHECK	APPROVE	DRAWING NO
C.B.LEE	W.Y.YANG	G.S.WEY	2028SCLZ (CPU) 1/1
07.05.28			

09.10

AVR154 CUP12030Z harman/kardon

JK43 CJJ2000BZ — CN46 CAP03A007Z — FROM INPUT B'D

CN47 — FROM INPUT --> DMP PCB — BN19 — FROM MCU B'D

TO DOWNLOAD JACK & OPTICAL IN B'D

FROM VIDEO3 JACK B'D — CN41 — V3 S-V Y, V3 S-V C, V3 COMP

JK40 CJJ9R003Z — VIDEO2, VIDEO1 OUT

JK41 CJJ9R001Z — VIDEO1 IN, DVD, MONITOR OUT

JK43(= JK42 + JK43 + JK49)	AVR-145	CJJ9R001Z
JK43(= JK42 + JK49)	AVR-245	CJJ9P003Z
JK40(= JK40 + JK41 + JK45)	AVR-145 & AVR-245	CJJ9R001Z

IC41 NJM2595M CVBS — IC42 NJM2595M S-C — IC43 NJM2595M S-Y

*NJM2595M OPTION ==>V_MUTE "LOW" ACTIVE

FUNC.	SW1	SW2	SW3	SW4	SW5
VIDEO1	L	H	X	X	H
VIDEO2	H	L	X	L	H
VIDEO3	H	H	H	H	H
V4_IPOD	H	H	X	L	H
DVD	H	H	L	H	H

*HCF4053M013TR OPTION

INPUT			*ON CHANNELS		
INH	C	B	A	C	B	A
H	X	X	X	NONE	NONE	NONE
L	L	L	L	CX	BX	AX
L	L	L	H	CX	BX	AY
L	L	H	L	CX	BY	AX
L	L	H	H	CX	BY	AY
L	H	L	L	CY	BX	AX
L	H	L	H	CY	BX	AY
L	H	H	L	CY	BY	AX
L	H	H	H	CY	BY	AY

HCF4053M013TR Connection Diagram

INPUT				"ON" CHANNELS		
INH	C	B	A	C	B	A
H	X	X	X	None	None	None
L	L	L	L	CX	BX	AX
L	L	L	H	CX	BX	AY
L	L	H	L	CX	BY	AX
L	L	H	H	CX	BY	AY
L	H	L	L	CY	BX	AX
L	H	L	H	CY	BX	AY
L	H	H	L	CY	BY	AX
L	H	H	H	CY	BY	AY

IC51 HCF4053M013TR — IC52 HCF4053M013TR — IC54 MM1511 — IC53 NJM2587V

* LC74763M OPTION TABLE

	C701	C702	X701
PAL	27P	27P	17.734
NTSC	33P	33P	14.318

IC71 LC74763M — IC72 74ACT04MTR

BN14 — FROM MCU B'D

CN45 — TO HDMI MUX B'D

JK62 — COMPONENT IN1, COMPONENT IN2 & COMPONENT OUT — EUR Ver. ONLY — 22P-->2P

IC61 NJW1321

JK69 — Pr_OUT, Pb_OUT, Y_OUT

CN43 — FROM REGULATOR B'D

MP — JE — ML — 2007.12.30

* DEFINITION OF I2C REGISTER (NJW1321)

I2C BUS FORMAT

MSB					LSB	MSB					LSB	MSB					LSB	
S(1BIT)	SLAVE ADDRESS(7BIT)					A(1BIT)	DATA(8BIT)					A(1BIT)	DATA(8BIT)					A(1BIT)	P(1BIT)

S : Starting Term
A : Acknowledge Bit
P : Ending Term

SLAVE ADDRESS

MSB	Slave Address(7BIT)						MSB	Hex
1	0	0	0	0	0	ADR(1BIT)	R/NOT W(1BIT)	--

R/NOT W : Set the Write Mode or Read Mode.
ADR : Set the Slave Address by " ADR" terminal.
R/NOT W = 0 : WRITE MODE, ADR = 0/1 ; ADR=0 Hex:94(h), ADR=1 Hex:96(h)
R/NOT W = 0 : READ MODE, ADR = 0/1 ; ADR=0 Hex:95(h), ADR=1 Hex:97(h)

CONTROL REGISTER TABLE
<WRITE MODE>

NO.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
DATA 1	PS1	PS2	OUT1			OUT2		
DATA 2	AUX0		AUX1		AUX2		AUX3	

PS : POWER SAVE
=> PS = 1 ; POWER SAVE ON (MUTE), PS = 0 ; POWER SAVE OFF (OUT ON)
OUT : OUTPUT
AUX : AUXILIARY (CONTROL SIGNAL OUTPUT)

<READ MODE>

NO.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
DATA	PORT0		PORT1		PORT2		PORT3	

PORT : INPUT

REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM — SHEET 5/6

MODEL: AVR154,AVR155/230

DESIGN	CHECK	APPROVE	DRAWING NO
S.H.Y	W.Y.Y	K.S.W	2030SCPZ (VIDEO) 1/1
07.12.30	07.12.30	07.12.30	

CUP12025Z

CUP12025-1 [FIP PCB]

CUP12025-5 [PHONE JACK PCB]
[PHONE/VID3(DIGITAL)]

CUP12025-6 [VR JACK PCB] [VR/HEAD PHONE&(MIC)/VID3(ANLOG)]

[KEY PCB] CUP12025-2

[STAND BY PCB]
CUP12025-3

[PWR.(MOMS)SW PCB]
CUP12025-4

CUP12025-8 [BLACKET JACK PCB FOR CARD CABLE]

CUP12025-9 [BLACKET JACK PCB FOR PHONE JACK]

FIP1 CFL17BT03GNK

IC73 HKVNL34H280A

IC75 74ACT04MTR

IC76 74HCU04AFN

IC86 NJM4556AL

IC87 NJM2068M

AVR254/354 ONLY

AVR154 ONLY

TO VR JACK PCB

TO INPUT ASS'Y

TO PHONE JACK PCB

FROM INPUT ASS'Y(MCU) CN72

FROM PHONE JACK PCB

FROM FIP PCB CN84

FROM MAIN ASS'Y CN86

TO VIDEO ASS'Y

BN81 TO POWER ASS'Y

REVISION	2		4		6	
1		3		5		7

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR154/254/354		1/7
DESIGN	CHECK	APPROVE	DRAWING NO
S.H.YANG	W.Y.YANG	G.S.WEY	2025SCDZ (FRONT)
07.12.07	07.12.07	07.12.07	1/1

LPP

ML 2007.12.07

	A	B	CH-SEL0	CH-SEL1	INPUT
0	L	L	H	H	HDMI2(CH-D)
1	L	H	H	L	NO USE
2	H	L	L	H	HDMI1(CH-C)
3	H	H	L	L	HDMI3(CH-A)

	INH	A	B	CH-SEL0	CH-SEL1	INPUT
0	L	L	L	H	H	HDMI2(CH-D)
1	L	L	H	H	L	NO USE
2	L	H	L	L	H	HDMI1(CH-C)
3	L	H	H	L	L	HDMI3(CH-A)
4	H	X	X	X	X	Z_NONE

HDMI_HPD_SELECT_BLOCK

HDMI_HPD_IN	HPD_DET	INH_LINE
L	L	H
H	H	L

RX	SEL1	SEL0
RX-A	LOW	LOW
RX-B	LOW	HIGH
RX-C	HIGH	LOW
RX-D	HIGH	HIGH

ADDRESS 0(pin103) : LOW
ADDRESS 1(pin128) : HIGH
ADDRESS 2(pin1) : LOW
ADDRESS 3(pin38) : LOW
ADDRESS 4(pin39) : HIGH
ADDRESS 5(pin64) : HIGH
ADDRESS 6(pin65) : LOW

Do not use

2007.08.0'

REVISION	2		4		6	
1		3		5		7

A

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR154/155		1/2
DESIGN	CHECK	APPROVE	DRAWING NO
M.S.K	W.Y.Y	K.S.W	2034SCDZ
07.03.29	07.03.29	07.03.29	(HDMI) 1/1

NOTE HIGHLIGHTED DIFFERENCES FOR MODEL AVR154,155

CUP12026Z

SR-CH

C-CH

BL-CH

* AVR154,155 : BL => SL

154=SL

FR-CH

SL-CH

FL-CH

EXCEPT AVR154/155

BR-CH

GAIN	R561, R562, R563, R564, R565, R850 R851
AVR154/155	1.8K
AVR255/355	1.6K

ONLY FAN USING

DC PROTECTOR

THERMAL PROTECTOR

OVERLOAD DETECTION

JW92: AVR154/155 ONLY

JK91

JK92

BN19

BN20

FOR USING FAN

EXCEPT AVR154/155

ONLY AVR154/155

AVR354/355 ONLY

AVR254/255/354/355 OPTION

AVR254/255/354/355 PART

FROM TRANS

AC IN

JW93, CL91, F902 : EXCEPT AVR154

FROM INPUT B'D

FROM TRANS B'D

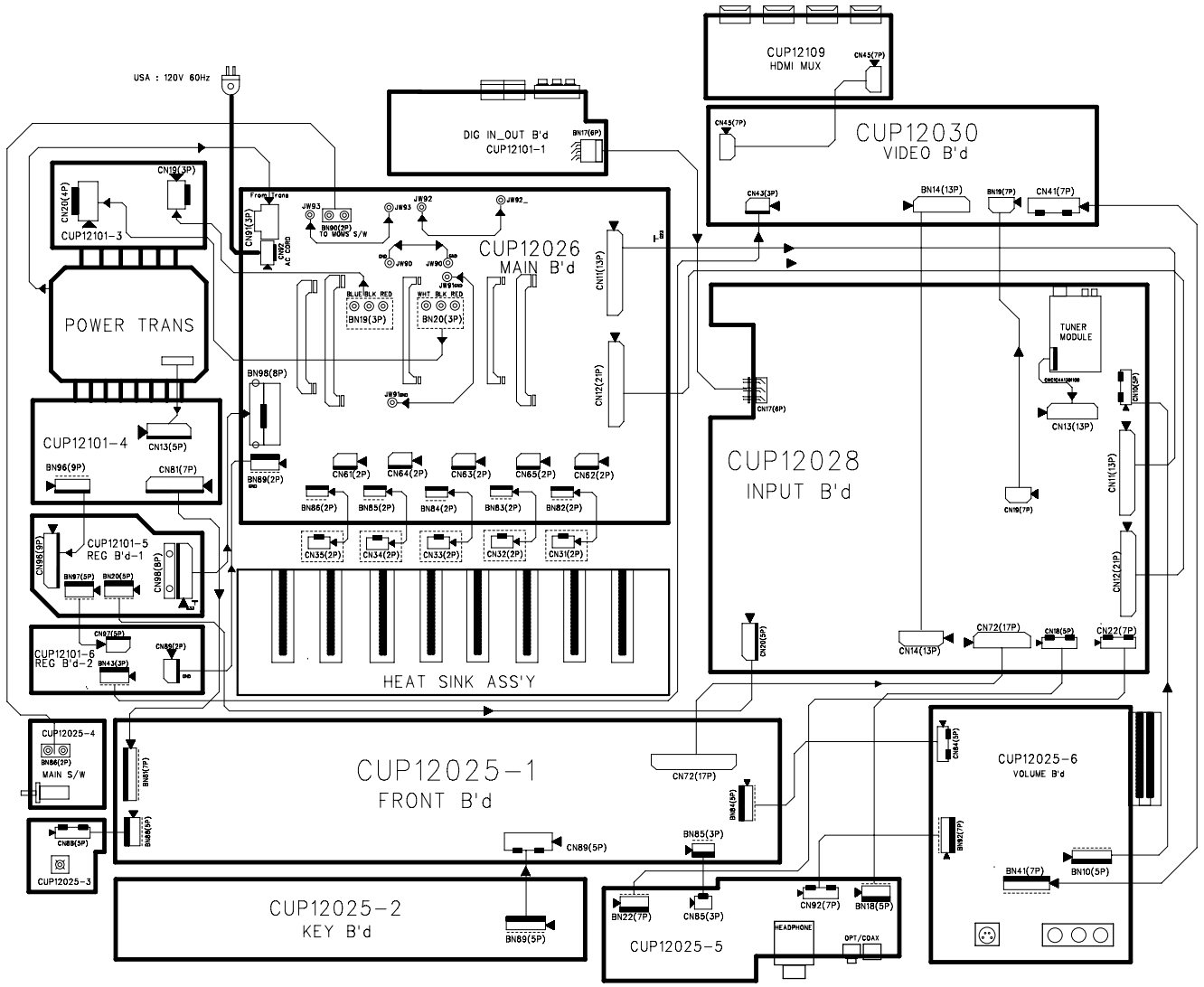
** IMPORTNAT SAFETY NOTICE.
INPORTANT FOR SAFETY WHEN REPLACING ANY OF THESE COMPONENTS
USE ONLY MANUFACTURE'S SPECIFIED PARTS.
** THE UNIT OF RESISTANCE IS OHM.
K=1000 OHM, M=1000 KOHM.
** THE UNIT OF CAPACITANCE IS MICROFARAD (uF)
pF = 10 ^ uF
** THIS SCHEMATIC DIAGRAM MAY MODIFIED AT ANY TIME WIHE THE
IMPROVEMENT OF PERFORMANCE.

DPP

ISSUE
2007.09.10

REVISION	1	2	3	SHEET
SCHEMATIC DIAGRAM				
MODEL	AVR154/155/254/255/354/355			2 / 7
DESIGN	CHECK	APPROVE	DRAWING NO	
C.B.LEE	W.Y.YANG	G.S.WEY	2026SCLZ (MAIN)	1 / 1
07.08.23				

AVR154 WIRING DIAGRAM



REVISION	2		4		6	
1		3		5		7

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR154		1/1
DESIGN	CHECK	APPROVE	DRAWING NO
J.T.B	W.Y.Y	K.S.W	WIRING DIAGRAM
08.03.11	08.03.11	08.03.11	1190SCDZ 1/1